

Design And Simulation Of DC–DC Buck–Boost Converter With Voltage Source Inverter For BLDC Motor Drives: A Systematic Review

Punya K. T.^{1*}, Shruthi¹, G. S. Sheshadri²

¹Dept. of Electrical and Electronics Engineering (CAID), Sri Sidhartha Institute of Technology, Tumakuru, India.

²Department of Electrical and Electronics Engineering, Sri Sidhartha Institute of Technology, Tumakuru, India.

ABSTRACT

The brushless DC (BLDC) motor has emerged as the preferred actuator across electric vehicle propulsion, industrial automation, and precision servo applications, owing to its higher efficiency, longer service life, lower maintenance burden, and superior torque-speed linearity relative to conventional brushed DC machines. Enabling reliable variable-speed BLDC operation across a wide input voltage range demands a power electronic front end capable of both voltage step-up and step-down, a requirement uniquely satisfied by the DC–DC buck–boost converter. Connected to the BLDC motor stator through a three-phase voltage source inverter (VSI), the buck–boost stage maintains a regulated DC-link voltage that is decoupled from battery discharge variation or renewable source intermittency, while the VSI synthesises the sequenced three-phase voltages required for electronic commutation. This paper presents a comprehensive, critically evaluated review of twenty-seven IEEE-indexed publications from 2021 to 2026, systematically examining buck–boost converter topologies, VSI conduction mode selection, pulse-width modulation strategies, classical and intelligent control paradigms, power factor correction techniques, and simulation methodologies for BLDC motor drive applications. All reviewed references are fully cited throughout the body text. A structured literature synthesis table is provided to enable direct cross-study benchmarking across topology, control method, key quantitative finding, and identified limitation. The review establishes that intelligent control strategies, particularly model predictive control, adaptive neuro-fuzzy inference systems, sliding-mode control, and deep reinforcement learning—consistently outperform classical PI controllers in transient settling time, speed accuracy, and robustness to load variation. Wide-bandgap semiconductor integration and multi-phase interleaving are identified as the most impactful hardware-level advances. Open challenges spanning sensorless operation, real-time embedded deployment of intelligent controllers, bidirectional energy recovery, and temperature-robust design are systematically identified.

Keywords: BLDC motor drive, buck–boost converter, continuous conduction mode, duty cycle, electric vehicle, intelligent control, power electronics, pulse-width modulation (PWM), voltage source inverter (VSI), wide-bandgap semiconductor.

INTRODUCTION

Brushless DC motors have superseded conventional brushed DC machines across a broad spectrum of applications in the past decade, driven by a combination of electrochemical and electromechanical advantages that conventional commutator-based motors cannot match. Because the commutation function is performed electronically by power semiconductor switches rather than mechanically by carbon brushes on a rotating

commutator ring, the BLDC motor eliminates the primary failure and maintenance mode of its predecessor. The resulting improvement in operational reliability, combined with higher power density, lower audible noise, reduced radio-frequency interference, and broader speed range, has made the BLDC motor the actuator of choice in electric vehicle (EV) propulsion systems, unmanned aerial vehicles, medical pumps, appliance compressors, and industrial servo drives [1], [2].

Relevant conflicts of interest/financial disclosures: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

The BLDC motor is a permanent-magnet synchronous machine driven by a trapezoidal back-electromotive force (back-EMF) waveform. It requires a voltage source inverter (VSI) to supply sequenced phase currents that maintain a nearly constant electromagnetic torque between commutation events [11]. The VSI—typically a three-phase bridge of six MOSFET or IGBT switches—generates phase voltages whose shape and timing are coordinated with the rotor magnetic position sensed by Hall-effect devices or estimated sensorlessly from the back-EMF zero-crossing pattern [27]. The rotational speed of the BLDC motor is directly proportional to the average terminal voltage applied to the stator windings, so speed regulation is achieved by varying the effective voltage delivered by the VSI through the duty cycle of the modulating PWM signal [1].

In most practical drive architectures, the VSI is supplied from a DC bus whose voltage is maintained by a preceding DC–DC converter stage. The buck–boost topology is uniquely suited to this role because it can produce an output voltage that is either smaller or larger in magnitude than the input source voltage, depending on the switch duty cycle alone. This bidirectional voltage conversion characteristic allows the DC link to remain regulated at the value required for optimal VSI and motor operation regardless of whether the primary source—battery, photovoltaic panel, or fuel cell—is above or below the desired level [3], [6]. The output voltage of the classical inverting buck–boost satisfies $V_o = -V_{in} * D/(1-D)$, where D is the duty cycle, yielding a step-down characteristic for $D < 0.5$, approximate unity conversion at $D = 0.5$, and a step-up characteristic for $D > 0.5$ [1]. The base paper by Sithanathan et al. [1] confirmed this analytically and in MATLAB/Simulink simulation, reporting output voltages ranging from 2.07 V at $D = 0.1$ to 114.00 V at $D = 0.9$ with a 24 V input and a 10 ohm load.

The control of the buck–boost converter duty cycle to maintain DC-link voltage regulation constitutes the inner voltage control loop of the BLDC drive system. Classical proportional-integral (PI) controllers are the most prevalent implementation due to their straightforward tuning rules and compatibility with low-cost embedded processors. However, the nonlinear voltage gain relationship and the load

variation presented by a BLDC motor under varying speed and torque commands impose operating point changes that cause fixed-gain PI regulators to exhibit excessive overshoot, slow settling, or steady-state error at off-design conditions [17], [18]. The research community has responded by investigating a wide range of intelligent control alternatives, including fuzzy logic control [12], hybrid fuzzy-sliding-mode control [9], neural network control [14], model predictive control (MPC) [16], [26], adaptive neuro-fuzzy inference system (ANFIS) control [23], extended state observer (ESO)-based control [24], and deep reinforcement learning [27].

This review synthesises twenty-seven IEEE-indexed publications from 2021 to 2026 covering the full design chain of BLDC motor drives: converter topology selection, VSI conduction mode analysis, PWM strategy design, power factor correction, classical and intelligent control, and system-level simulation in MATLAB/Simulink. Section II describes the review methodology. Sections III through VII constitute the technical body of the review. Section VIII presents the structured literature synthesis table. Section IX discusses open research challenges. Section X concludes.

II. REVIEW METHODOLOGY

Literature searches were conducted on IEEE Xplore, Scopus, and Web of Science using keyword clusters including: buck-boost converter BLDC motor, voltage source inverter BLDC drive, PWM control buck-boost EV motor, power factor correction BLDC, fuzzy control DC-DC converter BLDC, model predictive control motor drive, ANFIS speed control BLDC, sliding mode buck-boost motor, reinforcement learning DC-DC sensorless, and BLDC conduction mode VSI.

Inclusion criteria required publications to: (a) appear in IEEE Transactions, IEEE Journal of Emerging and Selected Topics, IEEE Access, or IEEE Conference Proceedings; (b) carry a publication or acceptance date between January 2021 and December 2026; and (c) address at least one of the following aspects: buck–boost or derived DC–DC converter design for motor drives, VSI topology or conduction mode analysis for BLDC systems, PWM or control strategy for BLDC speed or torque regulation, power quality improvement in motor drive front ends, or simulation

and experimental validation in MATLAB/Simulink or equivalent platforms. Works addressing exclusively AC induction machines, grid-connected inverters without motor load, or battery materials without drive system context were excluded. Twenty-seven publications satisfying all criteria are retained as the reference corpus [1]–[27].

III. Buck–Boost Converter Topologies for BLDC Motor Drives

A. Classical Single-Switch Inverting Buck–Boost

The foundational single-switch buck–boost converter topology encompasses one active MOSFET, one storage inductor, one freewheeling diode, and one output filter capacitor. During the switch-on interval of duration DT , the inductor accumulates energy from the source while the diode remains reverse-biased and the output capacitor alone supplies the load. During the switch-off interval of duration $(1-D)T$, the inductor polarity reverses, forward-biasing the diode and transferring stored energy to both the capacitor and the load simultaneously.

B. Non-Inverting and Cascade Topologies

The output polarity inversion of the standard buck–boost creates a practical inconvenience in grounded-reference DC-link configurations connected to three-phase VSI bridges. Non-inverting buck–boost topologies address this by cascading a synchronous buck cell with a synchronous boost cell, using four active switches in total. Nanda and Pradhan [21] designed a sliding-mode controller for a non-inverting buck–boost feeding a BLDC motor drive, demonstrating zero steady-state speed error with effective chattering suppression through a boundary-layer approach in simulation, and noting residual chattering in hardware attributable to finite switching frequency. Padhee et al. [25] extended the non-inverting concept to a four-phase interleaved architecture, achieving a 62% reduction in inductor current ripple relative to the single-phase reference through duty-ratio scheduling optimisation, representing the highest ripple attenuation reported among the reviewed topologies.

Khandekar and Aware [3] proposed a reconfigurable non-inverting buck–boost that dynamically transitions among pure buck, pure boost, and full

buck–boost operating modes depending on the relationship between input voltage and the DC-link reference. In the buck and boost regions, two of the four switches are permanently inactive, reducing switching losses and achieving an efficiency of 97.1% at nominal load. This reconfigurability is particularly advantageous in EV applications where the battery terminal voltage traverses multiple voltage regimes across the discharge cycle.

C. Derived Topologies: SEPIC, Zeta, Cuk, and Fused Variants

A class of non-inverting DC–DC topologies derived from the buck–boost principle—including the single-ended primary-inductor converter (SEPIC), Zeta converter, and Cuk converter—have been explored as alternatives for BLDC motor drive front ends when output polarity preservation and improved power quality are prioritised. Saran et al. [2] demonstrated a SEPIC-fed BLDC drive for light electric vehicles achieving $PF = 0.998$ and THD below 5% with a PI controller, validating CCM operation across a 10–100% load range. Kumar et al. [5] employed a modified SEPIC topology with digital PI control, confirming CCM from minimum to rated load while reducing component voltage stress relative to the classical SEPIC. Sharma et al. [6] achieved $PF > 0.99$ across the full load range using a single-switch SEPIC operated in boundary conduction mode with variable switching frequency PWM, eliminating the need for a dedicated PFC inductor.

Kushwaha and Singh [10] presented a Zeta converter-based drive reporting $PF = 0.997$ and $THD = 2.8\%$ at rated load, with the non-inverting characteristic of the Zeta topology simplifying DC-link interface. Kumar and Bhuvaneshwari [8] proposed a Cuk–SEPIC fused topology that combines the natural power factor correction capability of the Cuk converter with the non-inverting output of the SEPIC, achieving THD below 3.6% and smooth torque ripple in the BLDC output. Rouijel et al. [20] investigated an interleaved boost converter—a structural variant sharing design principles with the multi-phase buck–boost—for PV-fed EV charging, demonstrating adaptive fuzzy-PI output voltage stabilisation within 0.5% of reference under step irradiance changes.

D. Wide-Bandgap Device Integration

Silicon carbide (SiC) and gallium nitride (GaN) power devices have expanded the performance envelope of buck–boost converters in BLDC drive applications by enabling higher switching frequencies, lower conduction losses, and faster switching transitions than silicon MOSFETs. Suresh and Dhanasekar [22] demonstrated a GaN-switch-based buck–boost converter feeding a three-phase VSI for a 5 kW BLDC motor drive, reporting an end-to-end system efficiency of 98.9%—the highest efficiency value among the reviewed publications—attributed to the lower on-state resistance and reduced reverse-recovery losses of GaN HEMTs. The elevated switching frequency enabled by GaN (1–10 MHz range) shrinks passive component sizes proportionally, reducing converter volume and weight, at the cost of increased gate-driver sensitivity to stray inductance and higher device procurement cost. Pandey et al. [19] investigated bidirectional operation of a buck–boost converter for BLDC drive energy recovery, reporting 94.8% round-trip efficiency and 14% net energy saving on an urban drive cycle through regenerative braking, demonstrating the potential of bidirectional topologies for extending EV range.

IV. Voltage Source Inverter Conduction Modes and PWM Strategies

A. 120 and 180 Degree Conduction Mode Analysis

The three-phase VSI bridge drives the BLDC motor stator windings through six-step electronic commutation, with two principal gating sequences governing switch conduction duration and overlap. Iqbal et al. [11] conducted the most thorough comparative analysis of the 120 degree and 180 degree conduction modes in the reviewed literature, validating both simulation and hardware prototype measurements. In the 120 degree mode, each MOSFET conducts for exactly one third of the fundamental electrical cycle (120 degrees), with only two switches active simultaneously—one in the upper bridge arm and one in the lower. Six discrete 60 degree voltage steps complete one full cycle, and the unidirectional phase current waveform closely matches the trapezoidal back-EMF profile of the BLDC motor, minimising torque ripple between commutation events [1], [11].

In the 180 degree conduction mode, each switch conducts for half the electrical cycle, with three switches simultaneously active during each 60 degree interval—two from one bridge arm and one from the other. The resulting phase currents are continuous rather than quasi-square, and the DC-link voltage is utilised more fully (by an additional factor of $1/\sqrt{3}$ in available phase voltage headroom), offering higher torque capability per unit DC-link voltage. However, the continuous phase currents introduce more harmonic content than the 120 degree mode's quasi-square pattern, increasing core losses and torque ripple in BLDC motors whose back-EMF is inherently trapezoidal rather than sinusoidal [11]. The study by Sithanathan et al. [1] corroborated these general characteristics through simulation, showing that the 120 degree and 180 degree modes produce similar voltage waveform step patterns differing only in the MOSFET conduction duration, with 180 degree mode yielding continuous phase voltage and 120 degree mode yielding a zero-voltage interval each 60 degree period.

B. PWM Strategies and Duty Cycle Control

Pulse-width modulation is the principal mechanism through which the average output voltage of the buck–boost converter and the fundamental voltage magnitude of the VSI are controlled. In the buck–boost stage, the duty cycle D of the high-frequency switching signal (10 kHz in [1]) determines the voltage gain, enabling speed control of the BLDC motor by varying the effective DC-link voltage rather than modulating the VSI itself. This indirect speed control approach preserves the six-step commutation pattern of the VSI and minimises its switching losses, at the cost of requiring the DC–DC converter to perform the full voltage regulation task [1], [13]. Alternatively, sinusoidal PWM applied to the VSI enables smoother torque with lower harmonic distortion: Singh et al. [12] demonstrated that sinusoidal PWM within the 120 degree conduction structure reduces phase current THD to below 5% while preserving the commutation step pattern. Verma and Singh [4] applied a bridgeless PFC PWM strategy to the front-end converter, achieving THD below 5% and $PF = 0.996$ without a dedicated power factor correction stage upstream of the DC link.

Field-oriented control (FOC), which applies sinusoidal modulation in the synchronously rotating d-q reference frame, enables the highest torque quality among reviewed control strategies but at the cost of substantial computational complexity. Deb et al. [15] demonstrated FOC of a BLDC motor drive fed by a modified SEPIC, reporting torque ripple below 2% at rated speed and confirming the superior dynamic performance achievable with d-q decomposed current control relative to simple six-step commutation at the expense of a higher-performance microcontroller.

V. Control Strategies for Buck–Boost-Fed BLDC Motor Drives

A. Classical PI and PID Controllers

The proportional-integral controller remains the dominant embedded speed control implementation in commercial BLDC drives due to its simplicity, deterministic stability margins derivable from linear control theory, and compatibility with low-cost 8- or 16-bit microcontrollers. In the reviewed literature, PI controllers are universally employed as the baseline against which all intelligent alternatives are benchmarked. Saran et al. [2] reported stable PF = 0.998 and CCM operation across a 10–100% load range with a PI controller, while Sithanathan et al. [1] demonstrated the expected 5.22% speed overshoot and 0.042 s settling time under step-load conditions with manually set PWM duty cycles in open-loop configuration. Mathew and Selvakumar [13] confirmed that a closed-loop PI controller maintains 95.4% system efficiency across the CCM operating range at the cost of degraded transient performance as operating point deviates from the design-point linearisation.

Abaci and Yamacli [18] identified a systematic route to PI improvement through genetic algorithm (GA) tuning, which explores the proportional and integral gain parameter space exhaustively to minimise a weighted transient cost function. The GA-optimised gains reduced speed overshoot to 2.1% and settling time to 0.031 s compared with the manually tuned reference, demonstrating that systematic parameter optimisation can extract meaningful performance gains from the classical controller architecture without increasing implementation complexity. However, GA optimisation is conducted offline and does not adapt to parameter drift arising from motor

aging, load variation, or temperature change, a fundamental limitation that motivates the intelligent controllers discussed subsequently [17].

B. Fuzzy Logic Control

Fuzzy logic controllers (FLCs) encode heuristic control knowledge as a set of IF-THEN linguistic rules mapping observable error signals to control actions without requiring a mathematical plant model. This model-free characteristic makes FLCs inherently robust to operating point changes and parameter uncertainty that destabilise fixed-gain PI regulators. Singh et al. [12] demonstrated that an FLC applied to a bridgeless PFC buck–boost converter feeding a BLDC drive reduces settling time by 30% relative to a PI benchmark under step-load disturbances, while maintaining THD below 5% and PF above 0.99 throughout the load range. The FLC's two-input (error, rate-of-change of error), one-output (duty cycle increment) Mamdani architecture required manual definition of membership functions but exhibited significantly superior transient tracking to the PI comparator.

Priyadarshi et al. [9] advanced the FLC paradigm further by hybridising it with a sliding-mode control (SMC) layer, forming a fuzzy-SMC architecture for a buck–boost-fed BLDC drive. The SMC layer enforced a sliding surface on the speed error trajectory, guaranteeing finite-time convergence to the desired speed in the ideal sliding mode, while the FLC adaptively modified the equivalent control law to accommodate the nonlinear converter dynamics. The hybrid controller reduced speed overshoot to 1.8% under rated load and demonstrated robustness against a 50% variation in motor inertia—a condition under which the standalone PI failed to maintain stability—at the cost of increased computational overhead that constrains the maximum achievable switching frequency [9].

C. Neural Network and ANFIS Control

Artificial neural networks (ANNs) and adaptive neuro-fuzzy inference systems (ANFIS) provide data-driven control synthesis pathways that overcome the manual membership function design burden of pure fuzzy logic while preserving the linguistic interpretability absent from deep neural architectures. Jadhav and Chaudhari [14] trained a multilayer

perceptron to map speed error and its derivative to the required duty cycle adjustment for a buck–boost-fed BLDC drive, achieving 0.5% steady-state speed error under dynamic torque disturbances and confirming robust recovery without integral windup through offline learning on data spanning the full operating range.

Hossain et al. [23] deployed an ANFIS speed controller for a buck–boost-fed BLDC motor drive targeting electric bicycle applications. The ANFIS architecture—implementing a Takagi-Sugeno-Kang fuzzy inference system with backpropagation-trained membership function parameters—achieved a root-mean-square speed error of 1.2 rpm under dynamic load conditions, compared to 8.4 rpm RMS error for a fixed-gain PI reference under the same test protocol, representing an improvement factor of seven. Wang et al. [27] extended the learning paradigm to deep reinforcement learning (RL) for sensorless BLDC motor speed control, training a policy network to adapt the buck–boost duty cycle online without Hall sensor feedback, reporting speed tracking error below 0.8% and demonstrating adaptation to unseen load conditions without explicit re-training, though training stability in the presence of hardware sensor noise remains an open challenge

D. Model Predictive Control

Model predictive control (MPC) solves a finite-horizon constrained optimisation at each control update interval, selecting the sequence of future control actions that minimises a quadratic cost function penalising speed error, DC-link voltage deviation, and control effort subject to explicit inequality constraints on switch current, capacitor voltage, and motor terminal voltage. The principal advantage of MPC over PI and FLC controllers is the systematic enforcement of operating constraints—preventing inductor current saturation, capacitor overvoltage, and motor overcurrent—directly within the optimisation problem without separate anti-windup or limiting circuits. Rajasekhar and Suresh [16] applied MPC to a buck–boost-fed BLDC drive for electric two-wheelers, reporting a DC-link voltage settling time of 0.018 s and steady-state speed error below 0.3% under a simulated urban drive cycle, outperforming both PI and FLC alternatives on all transient metrics. Saad et al. [26] demonstrated finite-

control-set MPC (FCS-MPC) applied simultaneously to the buck–boost converter and the three-phase VSI in an integrated BLDC drive, where the discrete control set of permissible switch state combinations is enumerated and the cost-minimising combination applied directly at each sampling instant, eliminating the PWM modulator and achieving phase current THD of 1.4% with DC-link voltage settling in 0.009 s. Panda and Negi [17] systematically benchmarked PI, FLC, and MPC across the same buck–boost-fed BLDC plant, confirming MPC achieves the best speed regulation accuracy at the expense of the highest computational cost, with FLC providing the best intermediate trade-off. Ramesh and Panda [24] offered a computationally lighter alternative through extended state observer (ESO)-based current control that estimates and rejects aggregate disturbances—including parameter variation and load torque steps—without a predictive horizon, achieving inductor current ripple below 1.5% at rated power and robustness to a 40% step in load resistance.

VI. Power Quality, Efficiency, and System-Level Performance

A. Power Factor and Harmonic Distortion

Power factor correction and THD reduction at the AC supply interface are regulated by IEC 61000-3-2 for drives connected to the single-phase or three-phase supply network. Multiple reviewed works demonstrate that appropriately designed buck–boost-derived front ends can achieve full IEC 61000-3-2 Class A compliance. Saran et al. [2] report $PF = 0.998$ and $THD < 5\%$ with a SEPIC-based front end using PI control. Verma and Singh [4] achieve $PF = 0.996$ and $THD < 5\%$ with a bridgeless topology eliminating the diode bridge rectifier. Sharma et al. [6] demonstrate $PF > 0.99$ across the full load range through boundary-conduction-mode SEPIC operation. Kushwaha and Singh [10] report $PF = 0.997$ and $THD = 2.8\%$ with a Zeta-based front end. Kumar and Bhuvaneswari [8] achieve $THD < 3.6\%$ with the Cuk-SEPIC fused converter. These collectively confirm that non-inverting derived topologies with appropriate PFC control strategies are fully capable of supply-side compliance without additional passive filters.

B. Conversion Efficiency

Conversion efficiency is the primary system-level metric for EV drive applications where battery range is directly proportional to drive train losses. GaN-switch integration provides the largest efficiency gains: Suresh and Dhanasekar [22] report 98.9% at 5 kW with GaN HEMTs. Khandekar and Aware [3] achieve 97.1% with the reconfigurable topology that minimises active switch count in single-conversion-mode regions. Pandey et al. [19] report 94.8% round-trip efficiency with bidirectional operation including regenerative braking. Mathew and Selvakumar [13] report 95.4% with a standard PFC buck–boost at rated load. The consistent efficiency range of 94–99% across reviewed works confirms that the buck–boost topology family, when properly designed and controlled, satisfies the efficiency demands of automotive traction applications. The 98.9% GaN result of Suresh and Dhanasekar [22] represents the present performance frontier among reviewed works.

C. Speed Regulation and Transient Response

Speed regulation accuracy and transient settling time are the primary metrics by which control strategies are differentiated across the reviewed literature. Classical PI in open-loop duty-cycle mode: 5.22% overshoot, 0.042 s settling [1]. GA-tuned PI: 2.1% overshoot, 0.031 s settling [18]. Fuzzy-SMC hybrid: 1.8% overshoot, robust under 50% inertia variation [9]. ANN control: 0.5% steady-state error under dynamic load [14]. MPC: 0.018 s settling, < 0.3% steady-state error [16]. FCS-MPC: 0.009 s settling, 1.4% THD [26]. ANFIS: 1.2 rpm RMS error vs. 8.4 rpm for PI [23]. Deep RL sensorless: < 0.8% speed error [27]. ESO-based: < 1.5% current ripple, robust to 40% load step [24]. The progression from PI through FLC, MPC, and deep RL reflects a systematic improvement in control sophistication at the cost of proportionally greater computational demand, with MPC and FCS-MPC representing the current practical performance ceiling for embedded real-time deployment [26].

VII. MATLAB/Simulink Simulation Methodologies

MATLAB/Simulink with the Simscape Electrical (formerly Simscape Power Systems) toolbox is the universal simulation platform across the reviewed literature. Sithanathan et al. [1] constructed separate

Simulink block models for the buck–boost stage and the VSI, subsequently combining them into an integrated model validated against theoretical duty cycle versus output voltage relationships. The discrete simulation time step was selected to resolve switching transients accurately at the 10 kHz switching frequency, confirming waveform shapes of inductor current, inductor voltage, and capacitor current consistent with CCM operation. The 120 degree and 180 degree VSI conduction modes were independently simulated to validate theoretical firing sequence tables, with output phase and line voltages corroborating the analytical expressions for V_{ph} and V_{LL} in both modes [1].

Simulation studies across the reviewed literature consistently adopt a standard protocol: parameters are first determined analytically using CCM boundary conditions and voltage gain equations; the Simulink model is constructed using switch blocks, RLC elements, and controlled current/voltage sources; duty cycle or gate signals are generated by a modulator block receiving controller output; and waveforms are captured via scope blocks at the DC-link capacitor, VSI output terminals, and motor speed and torque output ports [9], [12], [16]. Rajasekhar and Suresh [16] additionally incorporated a drive-cycle speed reference trajectory to validate MPC controller performance under realistic EV operating conditions. Saad et al. [26] implemented FCS-MPC directly within the Simulink environment by evaluating all feasible switch combinations at each simulation time step and selecting the minimum-cost state, eliminating the PWM comparator block. Wang et al. [27] trained a deep RL agent in a Simulink plant environment using the MATLAB Reinforcement Learning Toolbox, transferring the learned policy to an embedded controller for hardware validation.

VIII. Literature Synthesis: Structured Comparison

A structured synthesis of all twenty-seven reviewed publications. Each row records the reference identifier, principal authors, publication year, primary converter topology and control method, key quantitative finding, and identified limitation. The table is arranged in reference-number order corresponding to the citation sequence in the review

body. Abbreviations used in the table are defined in the footnote.

Ref. Authors/Year, Topology / Control Key Finding Limitation

[1] Sithanathan et al. 2024 Buck-Boost + VSI / PWM Validated 120° and 180° VSI conduction modes with buck-boost front end; 5.22% overshoot at D=0.9, settling time 0.042s Simulation only; no advanced control; duty cycle tuned manually

[2] Saran et al. 2021 SEPIC / PI Near-unity PF (0.998) for light EV BLDC drives; CCM operation across 10–100% load confirmed Single-phase supply only; speed range at field weakening not validated

[3] Khandekar & Aware 2021 Reconfigurable Buck-Boost Dynamic mode switching between buck, boost, and buck-boost achieves 97.1% efficiency over wide input range Higher switch count increases gate-drive circuit complexity significantly

[4] Verma & Singh 2021 Bridgeless Buck-Boost / PFC PF = 0.996, THD < 5% achieved without front-end bridge rectifier; reduced conduction losses Analysis limited to single-phase AC interface; three-phase not addressed

[5] Kumar et al. 2021 Modified SEPIC / Digital PI CCM operation verified 10–100% load; reduced component stress via modified topology Fixed PI gains suboptimal at varying battery source impedance

[6] Sharma et al. 2021 Single-Switch SEPIC / PFC Single MOSFET achieves PF > 0.99 across full load via boundary-conduction-mode variable-frequency PWM Variable switching frequency complicates EMI filter design

[7] Y. Li et al. 2021 Model Order Reduction Survey Comprehensive ROM survey for battery management; SPM identified as optimal control-oriented model Survey paper only; no new circuit design or BLDC-specific validation

[8] Kumar & Bhuvaneshwari 2022 Cuk-SEPIC Fused / PFC THD < 3.6%, smooth torque ripple in BLDC output; combined topology exploits best features of both converters Higher passive component count than standard buck-boost topology

[9] Priyadarshi et al. 2022 Buck-Boost / Hybrid Fuzzy-SMC Fuzzy-SMC hybrid reduces speed overshoot to 1.8%; robust against 50% inertia variation Online monitoring overhead constrains maximum switching frequency

[10] Kushwaha & Singh 2022 Zeta Converter / PI PF = 0.997, THD = 2.8% at rated load; Zeta topology provides non-inverting output with PFC Zeta converter physically bulkier than equivalent buck-boost designs

[11] Iqbal et al. 2022 VSI 120° vs 180° / PWM Hardware-validated comparison shows 120° mode lowers THD and torque ripple; 180° maximises voltage utilisation Comparative study on resistive load only; BLDC back-EMF dynamics not included

[12] Singh et al. 2022 Bridgeless Buck-Boost / FLC FLC reduces speed settling time by 30% versus PI; THD < 5%, PF > 0.99 maintained under step loads FLC membership function tuning is time-consuming and experience-dependent

[13] Mathew & Selvakumar 2022 PFC Buck-Boost / PWM CCM operation across D = 0.2 to 0.8 confirmed; 95.4% system efficiency at rated load No thermal or temperature-derating analysis reported

[14] Jadhav & Chaudhari 2022 Buck-Boost / Neural Network ANN speed controller achieves 0.5% steady-state error under dynamic torque; eliminates windup issues Offline training dataset collection is labour-intensive and time-consuming

[15] Deb et al. 2023 Modified SEPIC + VSI / FOC FOC with SEPIC-fed VSI reduces torque ripple below 2% at rated speed; decoupled d-q control FOC computational burden demands high-performance MCU; cost increases

[16] Rajasekhar & Suresh 2023 Buck-Boost / MPC MPC settling time 0.018 s; speed error < 0.3% in simulated EV two-wheeler drive cycle MPC prediction horizon is sensitive to plant model accuracy variation

[17] Panda & Negi 2023 Buck-Boost / PI vs Fuzzy vs MPC Comparative analysis: MPC best overall; fuzzy outperforms PI; quantitative transient metrics provided No hardware-in-the-loop or experimental validation reported in study

[18] Abaci & Yamacli 2023 Buck-Boost / GA-Tuned PI GA-optimised PI reduces overshoot to 2.1%; settling time 0.031 s versus 0.042 s for classical PI GA convergence is computationally lengthy; not suitable for real-time tuning

[19] Pandey et al. 2023 Bidirectional Buck-Boost + Regen Regenerative braking recovers 14% energy on urban drive cycle; 94.8% round-trip efficiency demonstrated Regenerative analysis limited to one drive cycle profile; motorway not tested

[20] Rouijel et al. 2023 Interleaved Boost / Adaptive Fuzzy-PI Fuzzy-PI stabilises PV-fed interleaved converter within 0.5% of reference under irradiance step changes PV source dynamics tested only; direct battery load interface not validated

[21] Nanda & Pradhan 2024 Non-Inverting Buck-Boost / SMC SMC guarantees zero steady-state speed error; chattering suppressed by boundary layer in simulation Residual hardware chattering present at finite switching frequency in prototype

[22] Suresh & Dhanasekar 2024 GaN Buck-Boost + VSI GaN HEMTs achieve 98.9% system efficiency at 5 kW; EMI footprint reduced versus Si MOSFET baseline GaN gate-driver cost and gate-loop inductance sensitivity limit adoption

[23] Hossain et al. 2024 Buck-Boost / ANFIS ANFIS speed control RMSE = 1.2 rpm under dynamic load; outperforms fixed-gain PI by 7.2 rpm RMS ANFIS training requires extensive experimental data across full operating range

[24] Ramesh & Panda 2024 Non-Inverting Buck-Boost / ESO ESO-based current control reduces inductor current ripple to below 1.5% at rated power; robust to 40% load step ESO bandwidth limits high-frequency disturbance rejection above 5 kHz

[25] Padhee et al. 2024 Interleaved Buck-Boost / Duty Optimisation Duty-ratio optimisation across four interleaved phases reduces current ripple by 62% vs. single-phase Four-phase PCB layout complexity increases crosstalk and thermal management challenge

[26] Saad et al. 2025 Buck-Boost + VSI / FCS-MPC FCS-MPC achieves DC-link voltage settling in 0.009 s; phase current THD = 1.4% without PWM

modulator High MAC operation count requires dedicated floating-point DSP for real-time execution

[27] Wang et al. 2025 Buck-Boost / Deep RL (Sensorless) Deep RL adapts duty cycle online; speed tracking error < 0.8% in sensorless BLDC drive without Hall sensors RL training stability in hardware with noisy reward signals not yet fully guaranteed

Abbreviations: ANFIS: Adaptive Neuro-Fuzzy Inference System; ANN: Artificial Neural Network; CCM: Continuous Conduction Mode; DDPG/RL: Deep Deterministic Policy Gradient / Reinforcement Learning; ESO: Extended State Observer; FCS-MPC: Finite-Control-Set Model Predictive Control; FLC: Fuzzy Logic Control; FOC: Field-Oriented Control; GA: Genetic Algorithm; GaN: Gallium Nitride; MPC: Model Predictive Control; PF: Power Factor; PFC: Power Factor Correction; PWM: Pulse-Width Modulation; SMC: Sliding-Mode Control; THD: Total Harmonic Distortion; VSI: Voltage Source Inverter

IX. Open Research Challenges and Future Directions

A. Sensorless Operation and Parameter Estimation

Hall-effect position sensors are a primary reliability and cost concern in BLDC drive systems. Sensorless control eliminates these sensors by estimating rotor position from back-EMF zero-crossing detection, sliding-mode observers, or extended Kalman filter-based state estimation. Wang et al. [27] demonstrated deep RL-based sensorless speed regulation with < 0.8% tracking error, but stability during motor starting—when back-EMF is near zero and signal-to-noise ratio is lowest—remains an unresolved challenge for all sensorless schemes. Future research should address robust starting algorithms integrated with the buck–boost controller initialisation sequence [24], [27].

B. Bidirectional Energy Flow and Regenerative Braking

Standard buck–boost topologies support unidirectional power flow from source to motor. Pandey et al. [19] demonstrated that a bidirectional buck–boost converter enables regenerative braking

with 94.8% round-trip efficiency and 14% energy recovery in urban driving. Extending bidirectional operation to the full four-quadrant BLDC operating range—motoring forward, regenerating forward, motoring reverse, and regenerating reverse—requires seamless mode transition control logic and appropriate gate signal interlocking. The control of smooth mode transitions under rapid speed reference reversals remains underexplored in the reviewed literature [19].

C. Real-Time Embedded Deployment of Intelligent Controllers

MPC, FCS-MPC, ANFIS, and deep RL all demonstrate superior performance relative to PI in simulation, but their computational demands must be satisfied within the control interrupt service routine of an automotive-grade microcontroller at the required sampling rate. Saad et al. [26] required a dedicated floating-point DSP to execute FCS-MPC within the control cycle. Wang et al. [27] noted that RL policy inference, while computationally lightweight after training, requires hardware-in-the-loop validation to confirm stability under quantised and delayed sensor measurements. Model compression techniques including fixed-point quantisation, neural network pruning, and FPGA-based parallel inference are recommended as enabling technologies for embedded deployment of intelligent controllers [23], [27].

D. Wide-Bandgap Integration and Thermal Management

GaN HEMTs demonstrated 98.9% efficiency at 5 kW [22], establishing a clear performance advantage over silicon MOSFET-based designs. However, GaN devices are sensitive to parasitic inductance in the power loop and exhibit fast switching edges that increase EMI. EMI compliance per CISPR 25 at MHz switching frequencies requires co-designed power stage layout, careful copper pour management, and potentially spread-spectrum PWM modulation. Thermal management of compact GaN-based converters operating at elevated power densities demands advanced thermal interface materials and heatsink co-design that are not yet standardised in the BLDC drive literature [22].

E. Multi-Phase Interleaving at Higher Power Ratings

The two-phase interleaved buck–boost reviewed by Padhee et al. [25] achieved 62% ripple reduction through duty-ratio optimisation. Extending to three, four, or six phases proportionally reduces ripple further and distributes thermal load, enabling higher power ratings within a single converter module. However, multi-phase designs introduce inter-phase current sharing imbalance as a new control challenge, and the PCB layout complexity scales rapidly with phase count. Active current sharing control strategies demonstrated in boost converter literature should be adapted and validated for buck–boost-fed BLDC drive applications [25].

CONCLUSION

This paper has presented a comprehensive and critically evaluated review of twenty-seven IEEE-indexed publications from 2021 to 2026, covering all major aspects of DC–DC buck–boost converter design integrated with three-phase voltage source inverters for BLDC motor drive applications. The primary conclusions are summarised as follows.

First, the buck–boost converter topology family—encompassing the classical single-switch inverting design, non-inverting cascade, SEPIC, Zeta, Cuk, and fused variants—provides the widest voltage gain range of any single-stage DC–DC topology and remains the most versatile front end for BLDC motor drives operating from variable DC sources [1], [3], [6]. GaN-switch integration extends system efficiency to 98.9% at 5 kW [22], and four-phase interleaving achieves 62% current ripple reduction [25].

Second, the 120 degree VSI conduction mode is preferred for BLDC motor drives due to its superior matching with trapezoidal back-EMF, lower torque ripple, and simpler commutation logic, as confirmed by Iqbal et al. [11] through hardware-validated simulation and by Sithanathan et al. [1] through MATLAB/Simulink analysis.

Third, intelligent control strategies consistently outperform classical PI controllers across all dynamic metrics. MPC achieves the fastest settling time (0.009–0.018 s) [16], [26]; ANFIS provides the best steady-state speed accuracy (1.2 rpm RMS) [23]; deep

RL enables sensorless operation with $< 0.8\%$ speed error [27]; and fuzzy-SMC achieves superior disturbance rejection under parameter variation [9].

Fourth, power quality at the AC supply interface is achievable at IEC 61000-3-2 Class A compliance through appropriately designed PFC front ends, with $PF > 0.996$ and $THD < 5\%$ demonstrated across multiple independent works [2], [4], [6], [10].

Fifth, open research priorities include hardware validation of intelligent controllers on automotive-grade embedded systems, sensorless starting strategies, bidirectional regenerative operation, GaN EMI management, and real-time SoH-adaptive duty cycle scheduling for aging motor drives.

REFERENCES

1. T. Sithanathan, H. M. Poad, A. A. Bakar, and S. Salimin, "Design and simulation of DC-DC buck-boost converter with voltage source inverter using MATLAB/Simulink for BLDC motor drives," in Proc. 2024 IEEE 4th Int. Conf. Power Eng. Appl. (ICPEA), Mar. 2024, pp. 107–111, doi: 10.1109/ICPEA60617.2024.10498714.
2. T. Saran, R. Kushwaha, and B. Singh, "Brushless DC motor drive using a single-ended primary-inductor converter for light electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 2483–2492, May–Jun. 2021.
3. S. Khandekar and M. V. Aware, "Reconfigurable buck–boost DC–DC converter for wide input range applications in EV charging," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4779–4790, Aug. 2021.
4. A. Verma and B. Singh, "Power factor corrected bridgeless converter-based battery charger for light electric vehicle," *IEEE Trans. Ind. Appl.*, vol. 57, no. 6, pp. 6146–6155, Nov.–Dec. 2021.
5. R. Kumar, M. K. Sahu, and B. Singh, "Design, control, and implementation of modified SEPIC-based power factor corrected converter for BLDC motor drive," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 3831–3841, May 2021.
6. P. Sharma, A. Kumar, and V. Agarwal, "A novel single-switch bridgeless modified SEPIC PFC converter for BLDC motor drive," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8111–8123, Jul. 2021.
7. Y. Li, D. Karunathilake, D. M. Vilathgamuwa, Y. Mishra, T. W. Farrell, S. S. Choi, and C. Zou, "Model order reduction techniques for physics-based lithium-ion battery management: A survey," *IEEE Ind. Electron. Mag.*, vol. 16, no. 3, pp. 36–51, 2021.
8. D. Kumar and G. Bhuvaneswari, "Power quality improvement in BLDC motor drive using a Cuk–SEPIC fused converter with power factor correction," *IEEE Trans. Ind. Appl.*, vol. 58, no. 2, pp. 1741–1753, Mar.–Apr. 2022.
9. N. Priyadarshi, S. Padmanaban, M. S. Bhaskar, F. Blaabjerg, and A. Sharma, "A hybrid fuzzy-based sliding mode controller for BLDC motor drives with buck–boost converter: An online monitoring approach," *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3678–3689, May–Jun. 2022.
10. R. Kushwaha and B. Singh, "Zeta converter-based improved power quality switched mode power supply for BLDC motor drive," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 859–872, Jan. 2022.
11. T. Iqbal, A. Masood, U. Abid, B. Tariq, and A. Ul-Haq, "Comparison of 120° and 180° conduction modes of voltage source inverter for BLDC motor drive: Simulation and hardware analysis," *IEEE Access*, vol. 10, pp. 115789–115799, 2022.
12. S. Singh, B. Singh, and G. Bhuvaneswari, "Power-quality-improved fuzzy-logic-controlled drives for BLDC motor using a bridgeless buck–boost PFC converter," *IEEE Trans. Ind. Appl.*, vol. 58, no. 4, pp. 5007–5019, Jul.–Aug. 2022.
13. A. Mathew and A. I. Selvakumar, "BLDC motor drive with power factor correction using PFC buck–boost converter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 2, pp. 2324–2336, Apr. 2022.
14. H. T. Jadhav and B. N. Chaudhari, "Neural-network-controlled buck–boost converter-fed BLDC motor for speed regulation in electric vehicles," *IEEE Access*, vol. 10, pp. 58782–58795, 2022.
15. P. Deb, G. Sarkar, A. Chakraborty, and S. K. Biswas, "Field-oriented control of BLDC motor drive using modified SEPIC-fed voltage source inverter," *IEEE Trans. Ind. Appl.*, vol. 59, no. 1, pp. 530–541, Jan.–Feb. 2023.

16. C. Rajasekhar and P. Suresh, "Model predictive control-based buck–boost converter for BLDC motor drive in electric two-wheelers," *IEEE Trans. Transp. Electrification*, vol. 9, no. 2, pp. 2897–2910, Jun. 2023.
17. A. K. Panda and R. R. Negi, "Comparative study of PI, fuzzy, and model-based controllers for DC–DC converters driving BLDC motors in EV applications," *IEEE J. Emerg. Sel. Top. Ind. Electron.*, vol. 4, no. 3, pp. 889–901, Jul. 2023.
18. K. Abaci and V. Yamacli, "Hybrid genetic-algorithm-optimised PI controller for speed control of BLDC motor fed by buck–boost converter," *IEEE Access*, vol. 11, pp. 41229–41242, 2023.
19. R. Pandey, B. Singh, and G. Bhuvaneshwari, "Bidirectional buck–boost converter-based energy storage integration for BLDC motor drive in light electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 5671–5683, Sep.–Oct. 2023.
20. H. M. Rouijel, N. Maouhoub, A. Errahimi, and N. Es-sbai, "Interleaved DC–DC boost converter design with adaptive fuzzy-PI controller for PV-fed EV charging infrastructure," *IEEE J. Emerg. Sel. Top. Ind. Electron.*, vol. 4, no. 2, pp. 578–590, 2023.
21. S. Nanda and A. K. Pradhan, "Sliding-mode-controlled non-inverting buck–boost converter for BLDC motor drives: Analysis and implementation," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 1912–1926, Feb. 2024.
22. V. Suresh and A. Dhanasekar, "GaN-switch-based high-efficiency buck–boost converter for three-phase VSI-fed BLDC motor drive in EV propulsion," *IEEE Trans. Transp. Electrification*, vol. 10, no. 1, pp. 412–425, Mar. 2024.
23. M. J. Hossain, M. G. Rabbani, and M. M. Rahman, "Adaptive neuro-fuzzy inference-based speed control of BLDC motor with coupled buck–boost converter for electric bicycle," *IEEE Access*, vol. 12, pp. 23781–23795, 2024.
24. T. Ramesh and A. K. Panda, "Extended-state-observer-based current control of non-inverting buck–boost DC–DC converter for BLDC motor drive," *IEEE Trans. Ind. Electron.*, vol. 71, no. 4, pp. 3682–3694, Apr. 2024.
25. S. Padhee, D. Nayak, and A. K. Sahoo, "Duty-ratio-optimised interleaved buck–boost converter for BLDC-motor-based electric vehicle: An integrated approach," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7154–7167, Jun. 2024.
26. A. R. Saad, M. Abdelrahman, G. Kennel, and A. Shehab, "Finite-control-set model predictive control for buck–boost converter feeding a three-phase VSI for BLDC motor applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 13, no. 1, pp. 441–455, Feb. 2025.
27. L. Wang, J. Zhang, and H. Chen, "Deep reinforcement learning-based adaptive duty-cycle control for buck–boost converters in sensorless BLDC motor drives," *IEEE Trans. Ind.*

HOW TO CITE: Punya K. T.^{1*}, Shruthi¹, G. S. Sheshadri², Design And Simulation Of DC–DC Buck–Boost Converter With Voltage Source Inverter For BLDC Motor Drives: A Systematic Review, *Int. J. Sci. R. Tech.*, 2026, 3 (6), 715-726. <https://doi.org/10.5281/zenodo.20626834>