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Original Article

Digital Fault Detection and Self-Healing Circuit

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ABSTRACT

Modern digital circuits may experience faults due to aging, manufacturing defects, voltage fluctuations, and environmental disturbances. Conventional systems can require manual diagnosis and intervention, which may increase downtime. This paper presents a Digital Fault Detection and Self-Healing Circuit designed using Verilog Hardware Description Language (Verilog HDL). The proposed architecture contains a primary processing unit, a backup processing unit, a fault detection module, a Finite State Machine (FSM) controller, and a multiplexer (MUX). The fault detection module monitors system status. When a fault is detected, the FSM controller activates the backup processing unit, and the MUX selects the backup output. During fault-free operation, the primary processing unit remains active. The design is intended to improve system reliability and support continued operation when a detected fault occurs. Xilinx Vivado is identified for design, synthesis, and simulation, while ModelSim can be used for additional simulation and waveform inspection. Actual fault-detection accuracy, recovery time, hardware overhead, and reliability improvement must be evaluated through testbench simulation and, where applicable, hardware measurements.

Keywords: Digital Fault Detection, Self-Healing Circuit, Fault Tolerance, Verilog HDL, Finite State Machine, Multiplexer, Backup Processing Unit, Vivado

INTRODUCTION

Reliability is an important requirement in digital systems used in medical devices, automotive electronics, aerospace, and communication systems. Digital circuits can be affected by manufacturing defects, aging, voltage fluctuations, and environmental conditions. If a fault interrupts normal processing, the system may require diagnosis or repair before operation can continue.

The Digital Fault Detection and Self-Healing Circuit project proposes a design that detects a fault in the primary processing

unit and switches processing to a backup unit. A fault detection module provides a fault/no-fault indication. The FSM controller uses the status signal to control switching, while a MUX selects the output from the active processing unit. The design is described in Verilog HDL and is intended to be verified through simulation using Xilinx Vivado .

2. AIM AND OBJECTIVE

2.1 Aim

To design a Verilog HDL-based digital circuit that detects faults in a primary processing unit and switches to a backup processing unit using an FSM controller and a multiplexer.

2.2 OBJECTIVE

- Develop a primary processing unit for normal operation.
- Provide a backup processing unit to take over when a fault is detected.
- Design a fault detection module that generates a fault/no-fault status signal.
- Implement an FSM controller to manage switching between the primary and backup units.
- Use a MUX to select the active unit's output.
- Verify the design using simulation and testbench cases in Vivado or ModelSim.

3. SYSTEM REQUIREMENTS:

3.1 MODULE DESIGN

- Primary Processing Unit: performs normal computations when no fault is detected.
- Backup Processing Unit: takes over processing when the fault signal indicates a fault.

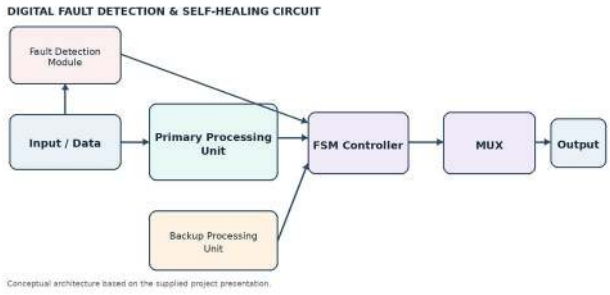
Relevant conflicts of interest/financial disclosures: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

- Fault Detection Module: monitors system status and indicates fault or no fault.
- FSM Controller: controls the transition between primary and backup operation.
- Multiplexer (MUX): selects which processing unit's data output is sent to the system output.
- Top Module: integrates the modules and coordinates control and data connections.

4.2 SOFTWARE REQIREMENTS

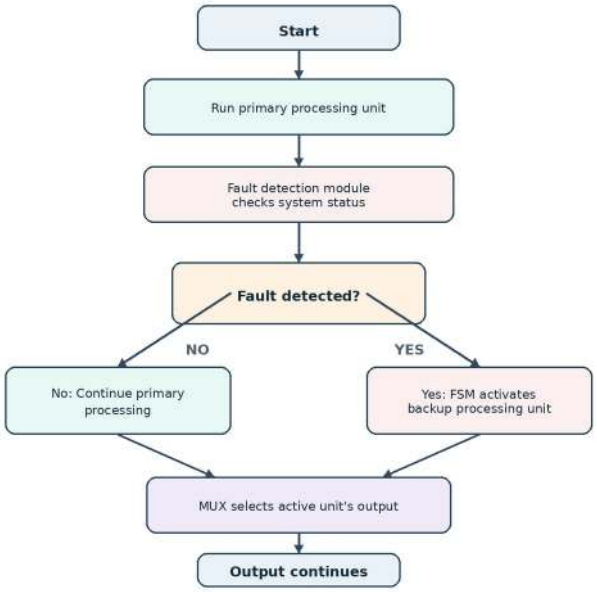
- Verilog HDL: describes the digital modules and control logic.
- Xilinx Vivado: used for design, synthesis, and simulation.

4 .BLOCK DIAGRAM

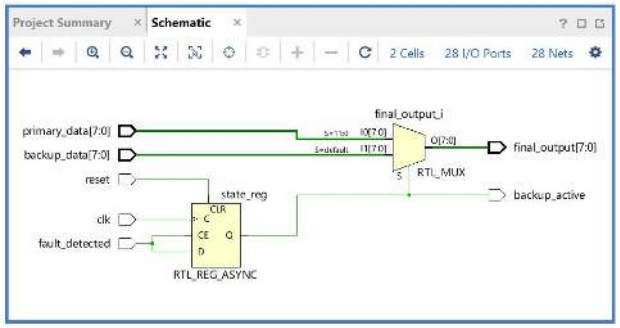


5. WORKING PRINCIPLE

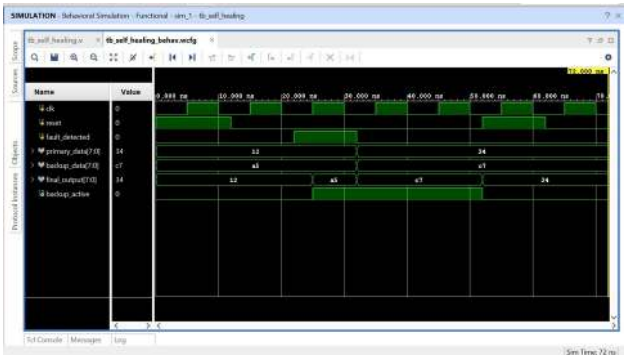
At startup, the system operates through the primary processing unit. The fault detection module continuously checks the defined system status. If no fault is indicated, the FSM keeps the primary unit selected and the MUX forwards its output. If a fault is detected, the FSM changes its control state and activates the backup processing path. The MUX then selects the backup unit's output. This process is intended to maintain output operation when the primary path experiences a detected fault. The exact behavior during recovery from a fault must be specified by the implementation.



6.CIRCUIT DIAGRAM



RESULT



8. ADVANTAGES

- Provides an automatic switching approach when a fault is detected.
- Offers a backup processing path for continued operation.
- Uses an FSM controller to coordinate fault response.
- Uses a MUX to select the active processing unit's output.

- Can be designed and verified with Verilog HDL simulation tools

a) ***Top of Form***

b) ***Bottom of Form***

9.APPLICATIONS

- Digital control systems requiring fault monitoring.
- Automotive electronic systems where reliability is important.
- Communication equipment requiring dependable processing.
- Aerospace and other systems where fault tolerance is a design concern.
- Educational and research prototypes for fault detection and recovery in digital circuits.

CONCLUSION

This paper presents a Digital Fault Detection and Self-Healing Circuit based on the project description supplied. The proposed system combines a primary processing unit, backup processing unit, fault detection module, FSM controller, and MUX. During normal operation, the primary unit supplies the output. When the fault detector indicates a fault, the controller selects the backup path and the MUX forwards its output. The design provides a structured approach to automatic fault response in digital systems. Further work should define the fault-detection method and processing-unit behavior, verify all switching cases through simulation, and report measured results before making quantitative claims about reliability or performance.

11.FUTURE SCOPE

Future development can define a specific fault model and implement detailed fault-detection logic for the chosen processing unit. The design can be extended with fault logging, status indicators, controlled recovery, and more than one backup path if the target application requires it. Testbenches can be expanded to cover transient faults, persistent faults, and repeated switching. FPGA implementation and synthesis analysis can be used to measure resource use, timing, and switching delay. These evaluations would help determine the practical reliability benefits and overhead of the self-healing approach.

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